

AACD 2026

March 18th – 20th

Advances in Analog Circuit Design

Programme Booklet

AACD 2026

March 18 – 20, 2026

Ulm, Germany



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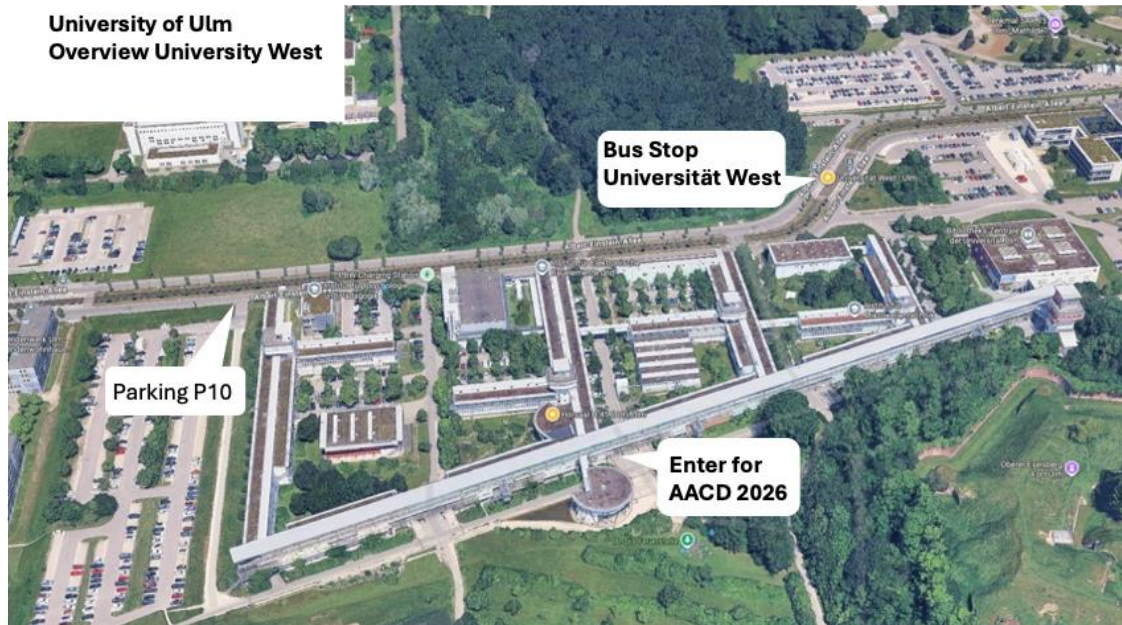


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Venue Information

AACD 2026 will take place at the **University of Ulm, Lecture Hall 45.2, Albert-Einstein-Allee 45, 89081 Ulm**. Signs around the vicinity will guide you to the entrance. You can use Google Maps to navigate to the building

<https://maps.app.goo.gl/D5VfKCa3YqHZkTK47>



Directions / Getting there

Construction areas: please note that there is a major construction going on in Ulm these days where the B10, one of the most important feeder roads, is closed in south direction. This also has an impact on local transport as well as on the general traffic situation. Major roads experience more jams than usual during rush hour.

International: Fly to Munich, Frankfurt or Stuttgart and take the train from there to Ulm.

Train system: We suggest to install the [DB Navigator app](#) for train connection planning. This app provides information about all train connections by *Deutsche Bahn*, whether local or long-distance. Alternatively, use www.bahn.de. We recommend taking high-speed long-distance trains, which are called “ICE – Intercity Express”. Book/buy train tickets before boarding the train. You can still purchase a ticket on board, but usually an extra fee applies.

By car: Coming from Munich or Stuttgart, leave the A8 motorway at the **Ulm West** exit in the direction of Ulm. Leave the motorway feeder road (**B10**) at the second exit “**Universität**”. At the next traffic light, turn left off **Berliner Ring** and turn into **Albert-Einstein-Allee**. Visitor

parking is available at **parking lot P10**, see <https://maps.app.goo.gl/QkbbHTAeQ3dTexAT8>. Please note that parking is often crowded.

Local transportation: The tram line S2 is usually the best option, but it is not currently running due to ongoing construction. From bus stations “**Hauptbahnhof**” or “**Theater**”, take **bus line 5** in the direction of **Science Park II/Wissenschaftsstadt**. The stop **Universität West** is about **200 m** from the workshop location. Google Maps can guide you there: <https://maps.app.goo.gl/D5VfKCa3YqHZkTK47>

Note: some hotels provide their guests with free public transportation tickets! Ask at the receptions!

Taxi/Uber: Most taxis park north of the train station. Uber is available in Ulm, too.

WiFi Access during the Workshop

All rooms allow Wi-Fi network access to *welcome* or *eduroam*.

Access to the free *welcome* Wi-Fi network does not require authentication. When using this network, you are responsible for encrypting your own security-relevant data.

eduroam is an international initiative for comprehensive internet coverage in educational institutions. After a one-time configuration at your home university, users receive internet access at all participating locations.

Conference Dinner

The conference dinner will take place Thursday evening, March 19th, in the Restaurant “Zur Lochmühle” in Ulm’s historic Fisherman’s Quarter:

<https://www.lochmuehle.com/en/>

Zur Lochmühle

Gerbergasse 6

89073 Ulm

You can use Google maps towards

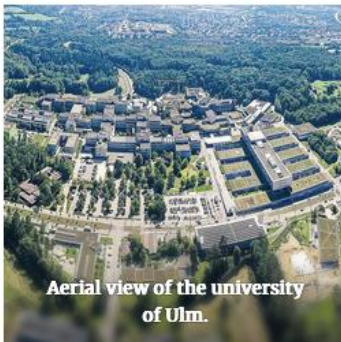
<https://maps.app.goo.gl/akyt3Wti5cLvi2WT8>



We will ask for dietary restrictions and provide a menu selection during registration.

Some Sights to see when in Ulm

Ulm is located in southern Germany between Stuttgart and Munich, with fast and easy connections from both cities and their airports. Frankfurt Airport is also linked to Ulm via high-speed train. Situated on the River Danube and surrounded by the scenic Swabian Alb, Ulm combines historic quarters with modern architecture, including the world's tallest historic church, the Ulm Minster. The Alps and Lake Constance are about an hour away, offering excellent opportunities for sightseeing, sports, and relaxation.



Aerial view of the university of Ulm.



University of Ulm: University west – library.



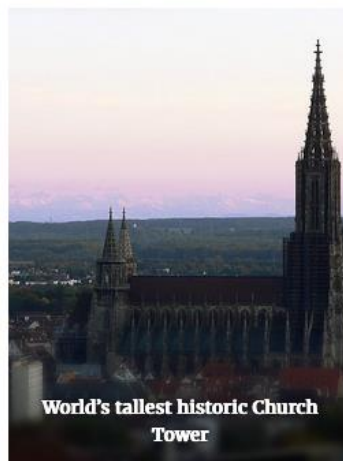
University of Ulm: Lecture hall 45.2



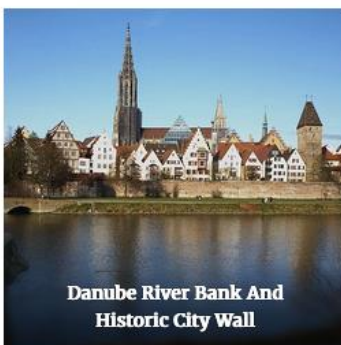
Ulm Fishermen's Quarter



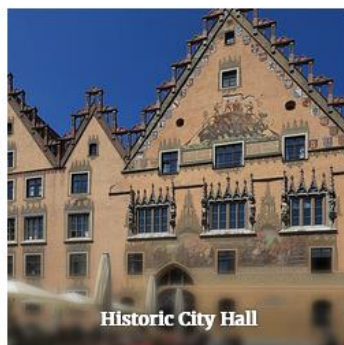
Conference Dinner Location



World's tallest historic Church Tower



Danube River Bank And Historic City Wall



Historic City Hall



Hotel „Schiefes Haus“

Programme Schedule

Wednesday March 18, 2026 Advances in High-Performance ADCs Chairman: Prof. Bram Nauta	
08:00	Registration
09:00	Opening ceremony
09:15	Wideband continuous-time ADCs for automotive applications Prof. Lucien Breems <i>NXP Semiconductors, The Netherlands</i>
10:00	High-Speed ADC Innovations: Architectures, Circuit Techniques & Calibration Prof. Pieter Harpe <i>Eindhoven University of Technology, The Netherlands</i>
10:45	Coffee break
11:15	High performance Noise-Shaping SAR ADCs Prof. Michael Flynn <i>University of Michigan, MI, USA</i>
12:00	High Linearity Delta-Sigma Analog to Digital Converters: From Discrete Time to Continuous-Time Architectures Dr. Francesco Conzatti <i>Infineon Technologies, Austria</i>
12:45	Lunch
13:45	Advances in High-Resolution Incremental ADCs Dr.-Ing. John G. Kauffman <i>University of Ulm, Germany</i>
14:30	Linearizing VCO-based ADCs Using A Pseudo-Virtual Ground Feedforwarding Technique Prof. Drew Hall <i>UC San Diego, CA, USA</i>
15:15	Coffee break
15:45	Welcome Address Prof. Michael Weber <i>President of University of Ulm, Germany</i>
16:00	Panel discussion

Thursday March 19, 2026
Sensor Interface Circuits
Chairman: Prof. Andrea Baschirotto

09:00 **Common-Mode Replication for High-Impedance Sensor Interfaces**
Prof. Qiang Li
Hamburg University of Technology, Germany

09:45 **Ultra-Low Power, High-Resolution Sigma-Delta Modulators for Multi-Sensor Platforms**
Prof. Piero Malcovati
University of Pavia, Italy

10:30 **Coffee break**

11:00 **Beyond Closed-Loop Architectures: Delivering High Performance in Power Constrained Gyroscopes**
Francesco Diazzi
Bosch Sensortec GmbH, Germany

11:45 **Echography System evolution and HV Ultrasound Drivers**
Giulio Ricotti
STMicroelectronics, Italy

12:30 **Lunch**

13:30 **Advanced Interface Circuits for Magnetic Sensors**
Johannes Janschitz
Infineon Technologies, Austria

14:15 **Time-to-Digital Converters for LiDAR and Advanced Sensing Applications**
Daniele Perenzoni
Sony Semiconductor Solutions Europe, Italy

15:00 **Coffee break**

15:30 **Panel discussion**

19:00 **Gala Dinner (Restaurant Zur Lochmühle)**

Friday March 20, 2026
High-Performance On-Chip References
Chairman: Prof. Kofi Makinwa

08:30	The Bandgap Reference: Achieving Stability in a Mass-Production World Brendan Whelan <i>Analog Devices, CA, USA</i>
09:15	Bandgap References: Recent Developments and Challenges in Nanometer CMOS Dr. Matthias Eberlein <i>Fraunhofer EMFT, Germany</i>
10:00	Coffee break
10:30	A Family of Simple Current References Based on 2T Voltage References Dr. Martin Lefebvre <i>TU Delft, The Netherlands</i>
11:15	A Sub-Ranging Current Reference with Process-Insensitive Second- Order TC Reduction Pangi Park <i>KAIST, South Korea</i>
12:00	Lunch
13:00	Hybrid LC/RC Frequency References Prof. Anne-Johan Annema <i>University of Twente, The Netherlands</i>
13:45	A High-Stability High-Accuracy RC Frequency Reference Karimeldean Mohamed <i>TU Delft, The Netherlands</i>
14:30	Panel discussion
15:30	End of Workshop

Programme Abstracts

Wednesday March 18, 2026

Advances in high-performance ADCs

Chairman: Bram Nauta



Wideband Continuous-time ADCs for Automotive Applications

Lucien Breems, NXP Semiconductors, The Netherlands

Abstract: Receivers used in automotive systems like terrestrial broadcast radio and radar-based ADAS depend on wideband analog-to-digital converters that deliver excellent linearity and high spectral purity. The continuous-time sigma-delta modulator fits the automotive receiver requirements very well, thanks to the inherent anti-alias filtering and high-gain feedback loop, but the maximum achievable bandwidth is limited by stability constraints. The continuous-time pipeline ADC architecture does not have this limitation, but its spurious performance depends on the (frequency dependent) matching accuracy between the analog and digital filters of the pipeline architecture. In this talk the latest cutting edge continuous-time sigma-delta and pipeline ADCs are presented that achieve better than 100dB SFDR in bandwidths up to several hundred MHz. The key architectural innovations, design challenges and calibration techniques are reviewed that enable this extreme performance.



High-Speed ADC Innovations: Architectures, Circuit Techniques & Calibration

Pieter Harpe, Eindhoven University of Technology, The Netherlands

Abstract: Applications such as communication continuously demand ADCs operating at higher speed (tens of GHz) while maintaining adequate energy efficiency. Making progress in this performance region is hampered by aperture limitations and auxiliary components like the input network and the clock drivers. Fortunately, technology scaling, hybrid ADC architectures, and advanced calibration methods have contributed to performance improvements. In this presentation, the main design challenges are reviewed, and recent state-of-the-art high-speed ADC examples are highlighted. The presentation will cover hybrid ADC architectures, innovative circuit techniques, calibration methods, and auxiliary circuits, all in the context of high-speed ADCs.



High-Performance Noise-Shaping SAR ADCs

Michael Flynn, University of Michigan, USA

Abstract: Abstract: Noise-shaping successive-approximation-register (SAR) ADCs offer excellent energy and area efficiencies. Researchers have introduced several techniques to improve bandwidth and resolution. Interleaving combines noise-shaping ADCs in parallel to increase bandwidth. The cascaded noise-shaping SAR architecture cascades multiple noise-shaping stages to provide high resolution, with a modest increase in area and power. In addition, the cascading significantly enhances robustness and eliminates the need for PVT calibration. A hybrid architecture adds a continuous-time frontend to provide many of the benefits of continuous-time $\Delta\Sigma$ modulators, and VCO-based front ends provide these advantages with a very small silicon footprint. Finally, incremental NS-SAR brings the benefits of noise shaping to high-resolution, Nyquist-rate conversion.

	<p>High Linearity Delta-Sigma Analog to Digital Converters: From Discrete Time to Continuous-Time Architectures</p>
	<p>Francesco Conzatti, Infineon Technologies, Austria</p>
	<p>Abstract: Analog to Digital Converters (ADC) are key components in several applications, for instance sensor interfaces, communication systems, radar sensing, just to name a few. ADC non-linearity leads to degraded performance at system level, for instance higher Bit-Error-Rate (BER), degraded Error Vector Magnitude (EVM) or audible artifacts (audio). Delta-Sigma-Modulators (DSMs) are proven to achieve very demanding linearity requirements and several techniques have been published in the State-of-the-Art in order to address DSM non linearities and in particular to linearize the feedback Digital to Analog Converter (DAC), which is the key component to guarantee overall signal fidelity. Dynamic Element Matching (DEM) is effective as a background linearization technique, but leads to an increase of both current consumption and loop delay. Another popular approach is calibrating the DAC, which complicates the ADC system integration and is often proposed as an off-chip background solution. Single-Bit DAC designs reach outstanding linearities, but their application is usually limited to low-speed and low-bandwidth scenarios. Recent works on Inherently Linear ADCs tackle these issues and propose converter architectures that do not need neither calibration nor DEM, but still can reach very competitive performance in terms of linearity for both low-speed and high-speed scenarios. In this context, this work will cover recent advancements on inherently linear Delta-Sigma ADCs, ranging from Discrete-Time (DT) to Continuous-Time (CT) architectures.</p>
	<p>Advances in high-resolution Incremental ADCs</p>
	<p>John G. Kauffman, University of Ulm, Germany</p>
	<p>Abstract: High-resolution, high-efficiency A/D converters are dominated by noise-shaping and oversampling architectures. However, in applications where true Nyquist-rate conversion is required, such as single-shot conversion, multiplexing, or time-interleaving, neither oversampling nor noise-shaping can be used. This is due to the very concepts that allow them to combine efficiency with performance, introduce memory into the system, and thus prevent sample-to-sample operation. This talk focusses on incremental delta-sigma ADCs as a solution to this. It combines Nyquist-rate conversion with high power efficiency. The theoretical background and state of the art (SoA) prototypes using dynamic reconfiguration techniques to reduce the impact of non-idealities on incremental A/D converters are reviewed. In particular, integrator slicing, variable bit-width (VBW), and recuperation phase (RP) are investigated based on several SoA implementations.</p>
	<p>Pseudo-Virtual-Ground Feedforward for Linear, High-Order VCO-Only $\Delta\Sigma$ ADCs</p>
	<p>Drew Hall, UC San Diego, USA</p>
	<p>Abstract: Time-domain $\Delta\Sigma$ ADCs that use VCOs as integrators scale cleanly in advanced CMOS, but their largely open-loop nature makes it hard to achieve both high linearity and higher-order noise shaping. This talk introduces pseudo-virtual-ground feedforward (PVG-FF), a technique that feedforwards the PVG residue to suppress VCO nonlinearity while enabling higher-order noise shaping with only a single feedback DAC. The result is a power-efficient ADC architecture with wide dynamic range and large input swing. A measured prototype achieves 92.1 dB SNDR over a 2.5 kHz bandwidth, 123 dB peak SFDR, and 1.8 Vpp differential input range, with verified robustness across supply and temperature.</p>

Thursday March 19, 2026

Sensor interface circuits

Chairman: Andrea Baschirotto



Common-Mode Replication for High-Impedance Sensor Interfaces

Qiang Li, Hamburg University of Technology, Germany

Abstract: Interfacing with high-impedance sensors, e.g., dry-contacted electrodes, accelerometers, etc., requires high CMRR with sufficient input impedance concurrently. The system CMRR is determined by the CMRR of the front-end amplifier as well as the imbalance of source impedance; the latter has to be accommodated by large input common-mode impedance. This talk presents a compact solution exploiting a dedicated CM loop which replicates the input CM voltage along with the DM signal, creating a unity-gain CM path which prevents any CM current flow, improving CMRR and input common-mode impedance simultaneously. A brief comparison between the CMR and traditional CMFB techniques will be discussed.



Ultra-Low Power, High-Resolution Sigma-Delta Modulators for Multi-Sensor Platforms

Piero Malcovati, University of Pavia, Italy

Abstract: The design of high-resolution ADCs for sensor applications is becoming quite challenging, since, with the advent of IoT applications the power budget is becoming extremely limited. This work presents a discrete-time, single-bit second-order Sigma-Delta Modulator (SDM), with 1-kHz bandwidth, a dynamic range (DR) larger than 110 dB, and a sampling frequency of 4 MHz, which exploits a number of specific techniques to minimize the power consumption. A prototype, integrated in a 65-nm CMOS technology, achieves a measured DR as large as 112 dB with a power consumption of only 240 μ W, of which only 163 μ W are static. The achieved Schreier figure-of-merit (FoM) of 178 dB is better than state-of-the-art SDM and competes with Zoom ADCs (FoMs around 180 dB), which, however, require a complex digital correction in order to reach an acceptable linearity.



Beyond Closed-Loop Architectures: Delivering High Performance in Power Constrained Gyroscopes

Francesco Diazzi, Bosch Sensortec GmbH, Germany

Abstract: The proliferation of consumer electronics, from smartphones and wearables to augmented reality systems, has established a roadmap for consumer-grade gyroscopes that is not only cost-effective but also operate with high power efficiency. This demanding market landscape continuously pushed evolutionary leaps in gyroscope architectures. We have witnessed a strategic transition from the historically automotive robust closed-loop systems to innovative open-loop designs. This architectural shift, however, has not come at the expense of crucial performance. Rather, it has necessitated ingenious engineering to maintain and even enhance the high-performance characteristics vital for accurate and reliable motion sensing across a myriad of applications. This system-level perspective will illustrate how choices made in the analog signal conditioning directly influence the requirements and capabilities of digital filtering and calibration, highlighting the necessity of a truly holistic and co-optimized design strategy.



Echography System evolution and HV Ultrasound Drivers

Giulio Ricotti, STMicroelectronics, Italy

Abstract: The talk begins with a technical introduction to the evolution of ultrasound echography systems, from preliminary images to 4D imaging techniques. It then provides an overview of 200 V silicon technology that enables high-voltage integrated circuit (HV IC) design for the transmission path. The presentation includes an analysis of pulse and linear driving, as well as high-voltage multiplexers, focusing on transmit (TX) beamforming. The talk concludes with a discussion of the design challenges involved in integrating thousands of high-voltage channels while maintaining very high signal quality and ultralow power requirements.



Advanced Interface Circuits for Magnetic Sensors

Johannes Janschitz, Infineon Technologies, Austria

Abstract: This presentation covers advanced magnetic sensor interface circuits for coreless current and position sensing, combining analog, digital, and digitally assisted signal processing to achieve high dynamic range, robustness against stray fields, and immunity to mechanical stress. A hybrid current sensor using coil and Hall paths is presented with multi-loop chopper ripple feedback that suppresses chopping artifacts, enabling a 10 MHz bandwidth with ~1% frequency-response flatness. Digital assisted signal processing ensures accurate ratiometric-to-VDD output, while analog/digital compensation corrects temperature and mechanical stress effects. Further interfaces include chopped continuous-time $\Sigma\Delta$ and hybrid ADCs for a dual-channel Hall sensor targeting functional safety, as well as a stray-field-robust Hall angle sensor. The angle sensor employs an orthogonal differential Sin/Cos Hall arrangement with a chopped, tracking continuous-time $\Sigma\Delta$ -ADC, local stress compensation, and digital multi-loop offset ripple feedback to maintain low output ripple under chopping. A linear Hall interface exploits an analog multiplying replica circuit to enforce precise ratiometric-to-VDD behavior together with mechanical stress and temperature compensation, combined with chopping/spinning and analog offset-ripple feedback loops for low-noise operation.



Time-to-Digital Converters for LiDAR and Advanced Sensing Applications

Daniele Perenzoni, Sony Semiconductor Solutions Europe, Italy

Abstract: This talk explores Time-to-Digital Converter (TDC) architectures and design considerations for direct Time-of-Flight (dTOF) LiDAR systems and related sensing applications. It provides insights into some of the analog and mixed-signal design challenges encountered in high-precision time measurement for consumer, automotive and industrial contexts. The discussion begins with an overview of TDC fundamentals and performance metrics such as resolution, DNL, INL, precision, and dynamic range. Various architecture approaches are then explored, including counter-based, current-starved delay lines, gated ring oscillators, and other topologies. Key design challenges are addressed, focusing on jitter sources, PVT robustness, and calibration strategies. SPAD integration aspects are also covered, including interface design considerations and event detection. Finally, applications ranging from automotive LiDAR and 3D imaging to proximity sensing and augmented reality are briefly examined. The talk includes examples from practical implementations and real-world design experiences, offering perspectives on developing TDC solutions for modern sensing systems.

Friday March 20, 2026

High-Performance On-Chip References

Chairman: Kofi Makinwa



The Bandgap Reference: Achieving Stability in a Mass-Production World

Brendan Whelan, Analog Devices, California, USA

Abstract: Precision measurement systems depend on the stability of the constituent components and circuit design over time and environmental conditions, which is often dominated by drift of a bandgap reference. This presentation will discuss theory of operation and root-cause of drift in bandgap references, with particular focus on the “soft” specs such as long-term drift, solder shift and thermal hysteresis. Foundational circuitry, various circuit architectures, and IC packaging will be reviewed, as well as system PCB design considerations. Difficulties in product manufacturing and test and current and future process trends will also be discussed.



Bandgap References: Recent Developments and Challenges in Nanometer CMOS

Matthias Eberlein, Fraunhofer EMFT, Germany

Abstract: This review surveys bandgap reference circuits from recent publications, highlighting advances in scaled CMOS and FinFET technologies. We examine solutions for achieving decent accuracy despite process variability, while emphasizing the limitations imposed by device models and temperature drift at sub-1 V supplies. Moving beyond classic bipolar-based schemes, the talk examines unconventional ways of achieving all-CMOS integration in modern SoC's. This includes techniques like weak-inversion, capacitive-bias and use of the bulk-diode. By discussing measured results and design tradeoffs, the presentation provides research directions for achieving robustness and high precision in advanced process nodes.



A Family of Simple Current References Based on 2T Voltage References

Martin Lefebvre, Delft University of Technology, The Netherlands



Abstract: The robustness of current and voltage references to PVT variations is essential to the operation of ICs in real-world conditions. However, while voltage references can meet most of these requirements with a handful of transistors, current references remain rather complex. In this talk, we will present a family of simple current references consisting of a two-transistor (2T) voltage reference, buffered onto a voltage-to-current converter by a single transistor. We will demonstrate with experimental results from four fabricated references that they are suitable for pA to μ A reference current generation, while also being PVT-robust and featuring low power and area overheads.



A Sub-Ranging Current Reference with Process-Insensitive Second-Order TC Reduction

Pangi Park, KAIST, South Korea

Abstract: Systems on Chip require stable current references to provide bias currents for analog blocks and define reference levels for current-domain ADCs. However, achieving a low temperature coefficient (TC) over a wide temperature range, while minimizing process-induced TC variation, is challenging due to the 2nd order TCs of most on-chip devices. This work presents a sub-ranging current reference that suppresses 2nd order TCs by combining a TC-adjustable current source and a process-insensitive sub-range detector. A prototype fabricated in 180-nm CMOS achieves a TC of 11.4 ppm/ $^{\circ}$ C over -20 to 125 $^{\circ}$ C, measured on 45 samples across five corner wafers.

	<p>Hybrid LC/RC Frequency References</p> <p>Anne-Johan Annema, University of Twente, The Netherlands</p>
	<p>A High-Stability High-Accuracy RC Frequency Reference</p> <p>Karimeldean Mohamed, Delft University of Technology, The Netherlands</p> <p>Abstract: Frequency references are key building blocks of most electronic systems. To allow other subsystems, e.g. transmitters or ADCs to reach their target performance, they must maintain their accuracy over Process, Voltage, Temperature and lifetime (PVTL). In this talk, the design of a hybrid LC/RC frequency reference will be presented. The main focus of the talk will be on the design of its LC oscillator, since this sets the accuracy and aging behavior of the whole system. It will be shown that the sensitivity of an LC oscillator to finite Q is fundamentally dependent on the chosen topology. By choosing the appropriate topology, and combining it with a low-power RC-based oscillator and a non-conventional temperature compensation scheme, the resulting hybrid frequency reference achieves state-of-the-art accuracy (~ 0.7ppm/K) over PVTL.</p> <p>Abstract: Modern electronic systems require stable frequency references for timing, synchronization, and communication. While crystal, BAW, and MEMS oscillators offer excellent stability, their co-integration with CMOS is difficult. RC-based references are fully CMOS-compatible, but their stability is limited by resistor temperature dependence and aging. This talk presents a high-stability 16MHz RC frequency reference implemented in a standard 180nm CMOS process. It consists of a frequency-locked loop, whose output frequency is locked to the time constant of a Wien bridge filter made from silicided resistors and MIM capacitors. A temperature compensation scheme based on a PNP-based temperature sensor results in ± 350ppm inaccuracy from -45°C to 85°C after a 2-point trim, which increases to only ± 450ppm after accelerated aging.</p>

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